



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,596	07/26/2001	Jun Koyama	12732-056001	7197
26171	7590	10/23/2003	EXAMINER	
FISH & RICHARDSON P.C. 1425 K STREET, N.W. 11TH FLOOR WASHINGTON, DC 20005-3500			NGUYEN, KEVIN M	
			ART UNIT	PAPER NUMBER
			2674	
DATE MAILED: 10/23/2003				

6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/912,596	KOYAMA, JUN
Examiner	Art Unit	
Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 26 July 2001.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-45 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 3-7,20,22,23,25,26,28,29,31,32,34,35,37,38,44 and 45 is/are allowed.

6) Claim(s) 1,2,8-19,21,24,27,30,33,36 and 39-43 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

 1. Certified copies of the priority documents have been received.

 2. Certified copies of the priority documents have been received in Application No. _____.

 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

 a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2,5</u> .	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Drawings

1. Figures 13, 14, 19A, 19B, 20A, 20B, 20C, 20D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Bell et al (US 4,996,523).

As to claim 1, Bell et al teaches a light-emitting device having a plurality of pixels (40), at least one pixel is driven by a memory cell (22) (see figure 1, column 3, lines 1-9).

4. Claim 1, 2, 10-13, 27, 30, 33, 36, 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Okumura et al (US 5,945,972).

As to claim 1, Okumura et al teaches a light-emitting device having a plurality of pixels (410), at least one pixel is driven by memory circuits (PM1, PM2) (see figure 21, column 24, lines 26-45 and column 28, lines 4-11).

As to claim 2, Okumura et al teaches a light-emitting device having a plurality of pixels (410), at least one pixel is driven by $n \times m$ memory circuits (PM1, PM2) for storing n -bits digital image signals for m frames (see figure 21 and 25, column 24, lines 26-45, column 26, lines 32-48 and column 29, lines 4-11).

As to claims 10, 27, Okumura et al teaches DRAM (column 18, line 23).

As to claims 11, 30, Okumura et al teaches inherently the memory circuits are formed over a glass substrate.

As to claims 12, 33, Okumura et al teaches the light-emitting device is an electro-luminescence display device (column 28, lines 9).

As to claims 13, 36, Okumura et al reviews the light-emitting device is incorporated in portable personal computers, hand-held terminals, portable TV sets, cellular phones, electronic notebooks, game machines, etc. (column 2, lines 15-20).

As to claim 43, Okumura et al teaches a light-emitting device having a plurality of pixels (410), at least one pixel is driven by $n \times m$ memory circuits (PM1, PM2) for storing n -bits digital image signals for m frames, where $m > 1$ (see figure 21 and 25, column 24, lines 26-45, column 26, lines 32-48 and column 29, lines 4-11).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8, 9, 21, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al in view of Nakamura (US 6,563,480).

As to claims 8, 9, 21, 24 Okumura et al teaches all of the claimed limitation of claim 1, except for SRAM and FeRAM. However, Nakamura teaches SRAM and FeRAM (column 2, lines 53-54). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the SRAM and FeRAM taught by Nakamura for Okumura et al's display system because this would reduce occupied area and capable of operating at a higher speed, while fabricating a display panel at low cost (column 1, lines 39-41 of Nakamura).

7. Claims 14, 18-19, 15, 39, 41, 16, 40, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al in view of Saito et al (US 6,366,026).

As to claims 14-16, Okumura et al teaches a light-emitting device associated with a method having a plurality of pixels (CEL), at least one pixel is driven by memory cell (PM1, PM2), writing the n-bit digital image signals from the source signal line (411) into memory circuits (PM1, PM2) at a row (412) where the gate signal line is selected; reading out the n-bit digital image signals stored in the memory circuits (PM1, PM2) in each of the plurality of pixels (CEL) (see figure 21, column 24, lines 27-45). Okumura et al fails to teach inputting the sampling pulses into latch circuits, holding the digital image signals in accordance with the sampling pulses in the latch circuits. However, Saito et al teaches outputting sampling pulses from shift register circuits (30); inputting the sampling pulses into latch circuits (31), holding the digital image signals in accordance with the sampling pulses in the latch circuits (33) (figure 4, column 6, lines 36-58). It

would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the latch circuit (31) and holding circuit (33) taught by Saito et al for Okumura et al's display device because this would improve the quality of the image being display, while fabricating the driving circuitry at reduced power dissipation (column 2, lines 32-36 of Okumura et al).

As to claim 17, Okumura et al teaches in a display period of a still picture "frame n to frame n+5", the n-bit digital image signals stored in the memory circuits are repeated read out to display the still picture "frame n to frame n+5", and the source signal line driver circuits is stopped (figure 25, column 26, lines 32-48).

As to claims 18, 39, 40, Okumura et al teaches the light-emitting device is an electro-luminescence display device (column 28, lines 9).

As to claims 19, 41, 42, Okumura et al reviews the light-emitting device is incorporated in portable personal computers, hand-held terminals, portable TV sets, cellular phones, electronic notebooks, game machines, etc. (column 2, lines 15-20).

Allowable Subject Matter

8. Claims 3, 5, 6, 22, 25, 28, 31, 34, 37, 44, 4, 7, 20, 23, 26, 29, 32, 35, 38, 45 are allowed.

9. The following is an examiner's statement of reasons for allowance: Okumura et al teaches a EL display device including a source signal line (411), n writing and reading gate signal lines (412), n writing transistors (426), n reading transistors (427), n x m memory circuits (PM1, PM2), n writing memory circuit selection portions (421), n reading memory selection portions (422) (see figures 21 and 25, column 24, lines 26-

45, column 26, lines 32-48 and column 29, lines 4-11). Accordingly, the cited prior arts do not teach or fairly suggest electroluminescence display device including a source signal line, n (n is a natural number, $n \geq 2$) writing and reading gate signal lines, n writing transistors, n reading transistors, $n \times m$ memory circuits for storing n bit digital signals for m frames (m is a natural number, $m \geq 1$), n writing memory circuits selection portions, n reading memory selection portions; the EL driving transistor, one of a source region and a drain region of the EL driving transistor is electrically connected to the current supply line, and the other of the source region and the drain region of the EL driving transistor is electrically connected to one electrode of the EL element. These distinct features have been added to the independent claims and render the above limitations are allowable.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
October 15, 2003



RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600